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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,708	06/27/2003	Per Hammarlund	42P16351	9639

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EXAMINER	
CERULLO, JEREMY S	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,708	HAMMARLUND ET AL.	
	Examiner	Art Unit	
	Jeremy S. Cerullo	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 are pending in this office action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 13-14, 18-19, and 22-25 are rejected under 35 U.S.C. 102(e) as being anticipated by of U.S. Patent No. 6,493,741 ("Emer" et al.).

4. As for Claim 1, Emer discloses monitoring a node associated with a contended lock (address of a lock is equivalent to the node associated with a contended lock; Column 5, Line 28 – Column 6, Line 11), and putting a processor waiting for a lock to sleep until an event occurs at the lock address (placing a TPU into a quiesce mode is equivalent to putting it to sleep; Column 5, Line 62 – Column 6, Line 11).

5. As for Claims 2 and 3, Emer further discloses the use of pair of instructions (LDx_ARM and QUIESCE) in order to halt a processor (put it to sleep) while it waits for

an event to occur (Column 5, Lines 28-40). LDx_ARM and QUIESCE are functionally equivalent to the claimed instructions, MONITOR and MWAIT.

6. As for Claim 4, Emer also discloses in Column 6, Lines 55-60, that the awakened processor acquires the resource after the resource is available.

7. As for Claims 13-14, in Column 5, Line 28 – Column 6, Line 11, Emer discloses a processor (Figure 2, Item 100) with logic that allows the address of a lock (equivalent to the node associated with a contended lock) to be monitored, the monitoring comprising detection of the lock becoming available. Emer also discloses that a Thread Processing Unit (a logical processor) is put to sleep while waiting for lock until an event occurs at the lock address. Emer further discloses the use of pair of instructions (LDx_ARM and QUIESCE) in order to halt a processor (put it to sleep) while it waits for an event to occur (Column 5, Lines 28-40). LDx_ARM and QUIESCE are functionally equivalent to the claimed instructions, MONITOR and MWAIT.

8. As for Claims 18-19, in Column 5, Line 28 – Column 6, Line 11, Emer discloses a system with a storage medium (Figure 2, Item 137) and a processor coupled with the storage medium (Figure 2, Item 100) with logic that allows the address of a lock (equivalent to the node associated with a contended lock) to be monitored, the monitoring comprising detection of the lock becoming available. Emer also discloses that a Thread Processing Unit (a logical processor) is put to sleep while waiting for lock until an event occurs at the lock address. Emer further discloses the use of pair of

instructions (LDx_ARM and QUIESCE) in order to halt a processor (put it to sleep) while it waits for an event to occur (Column 5, Lines 28-40). LDx_ARM and QUIESCE are functionally equivalent to the claimed instructions, MONITOR and MWAIT.

9. As for Claim 22, in Column 5, Line 28 – Column 6, Line 11, Emer discloses a method in which the address of a lock (equivalent to the node associated with a contended lock) is monitored. Emer also discloses that a processor is put to sleep while waiting for lock until an event occurs at the lock address. Emer also discloses in Lines 55-60 of Column 6 a set of instructions to perform these actions. It is inherent that in order for the computer to execute these instructions, they must be stored on a computer-readable medium.

10. As for Claims 23 and 24, Emer further discloses the use of pair of instructions (LDx_ARM and QUIESCE) in order to halt a processor (put it to sleep) while it waits for an event to occur (Column 5, Lines 28-40). LDx_ARM and QUIESCE are functionally equivalent to the claimed instructions, MONITOR and MWAIT.

11. As for Claim 25, Emer also discloses in Column 6, Lines 55-60, that the awakened processor acquires the resource after the resource is available.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claims 5 and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emer in view of U.S. Patent Application Publication No. 2003/0236816 (Venkatasubramanian, "Ven").

15. As for Claim 5, Emer teaches the limitations inherited from Claim 1 (See rejection above), but Emer does not teach that the processor is in a queue awaiting the release of the locked resource. However, in Paragraph [0003] on Page 1, Ven does teach the use of a sleep queue for threads waiting for a lock. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used a queue as taught by Ven in the method of Emer in order to allow processors access to the resource in the order they requested it, preventing starvation of the sleeping processor.

16. As for Claims 9-12, Emer and Ven teach a queue of processors awaiting the release of a monitored, locked resource, such that the next processor on the queue acquires the lock upon its release (See rejection of Claim 5 above). Emer further teaches the use of pair of instructions (LDx_ARM and QUIESCE) in order to halt a processor (put it to sleep) while it waits for an event to occur (Column 5, Lines 28-40). LDx_ARM and QUIESCE are functionally equivalent to the claimed instructions, MONITOR and MWAIT.

17. Claims 6-7, 15-16, 20-21, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emer in view of U.S. Patent No. 6,035,374 ("Panwar" et al.).

18. As for Claim 6, Emer teaches all of the limitations inherited from Claim 1, but Emer does not teach that putting a processor to sleep comprises the processor relinquishing all of its resources. However, Panwar teaches that a sleeping virtual processor must release its resources to allow them to be used by other virtual processors (Column 8, Lines 33-44). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the processor of Emer release its resources as taught by Panwar in order to prevent itself from interfering with the execution of instructions for the other virtual processors (Panwar: Column 8, Lines 41-44).

19. As for Claim 7, Emer teaches all of the limitations inherited from Claims 1 and 4. Emer also teaches in Lines 1-11 of Column 6 that when the TPU changes to a non-quiesce mode (awakens), the event monitor is disarmed. Emer does not teach that the

processor uses relinquished resources. However Panwar teaches that a sleeping virtual processor must release its resources to allow them to be used by other virtual processors (Column 8, Lines 33-44). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the processor of Emer release its resources as taught by Panwar in order to prevent itself from interfering with the execution of instructions for the other virtual processors (Panwar: Column 8, Lines 41-44). This also means that when a processor awakens, the resources it uses have been released (relinquished) by other processors.

20. As for Claim 15, Emer teaches all of the limitations inherited from Claim 13, but he does not teach that putting a processor to sleep comprises relinquishing of resources. However, Panwar teaches that a sleeping virtual processor must release its resources to allow them to be used by other virtual processors (Column 8, Lines 33-44). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the processor of Emer release its resources as taught by Panwar in order to prevent itself from interfering with the execution of instructions for the other virtual processors (Panwar: Column 8, Lines 41-44).

21. As for Claim 16, Emer teaches all of the limitations inherited from Claim 13. Emer also teaches in Lines 1-11 of Column 6 that when the TPU changes to a non-quiesce mode (awakens), the event monitor is disarmed. Emer does not teach that the processor uses relinquished resources. However Panwar teaches that a sleeping virtual processor must release its resources to allow them to be used by other virtual processors (Column 8, Lines 33-44). It would have been obvious to one of ordinary skill

in the art at the time of the invention to have the processor of Emer release its resources as taught by Panwar in order to prevent itself from interfering with the execution of instructions for the other virtual processors (Panwar: Column 8, Lines 41-44). This also means that when a processor awakens, the resources it uses have been released (relinquished) by other processors.

22. As for Claim 20, Emer teaches all of the limitations inherited from Claim 18, but he does not teach that putting a processor to sleep comprises relinquishing of resources. However, Panwar teaches that a sleeping virtual processor must release its resources to allow them to be used by other virtual processors (Column 8, Lines 33-44). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the processor of Emer release its resources as taught by Panwar in order to prevent itself from interfering with the execution of instructions for the other virtual processors (Panwar: Column 8, Lines 41-44).

23. As for Claim 21, Emer teaches all of the limitations inherited from Claim 18. Emer also teaches in Lines 1-11 of Column 6 that when the TPU changes to a non-quiesce mode (awakens), the event monitor is disarmed. Emer does not teach that the processor uses relinquished resources. However Panwar teaches that a sleeping virtual processor must release its resources to allow them to be used by other virtual processors (Column 8, Lines 33-44). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the processor of Emer release its resources as taught by Panwar in order to prevent itself from interfering with the execution of instructions for the other virtual processors (Panwar: Column 8, Lines 41-

44). This also means that when a processor awakens, the resources it uses have been released (relinquished) by other processors.

24. As for Claim 26, Emer teaches all of the limitations inherited from Claim 22, but Emer does not teach that putting a processor to sleep comprises the processor relinquishing all of its resources. However, Panwar teaches that a sleeping virtual processor must release its resources to allow them to be used by other virtual processors (Column 8, Lines 33-44). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the processor of Emer release its resources as taught by Panwar in order to prevent itself from interfering with the execution of instructions for the other virtual processors (Panwar: Column 8, Lines 41-44).

25. Claims 8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emer and Panwar as applied to Claims 6 and 15 above, and further in view of U.S. Patent Application Publication No. 2003/0126186 ("Rodgers" et al.).

26. As for Claim 8, Emer and Panwar teach all of the limitations inherited from Claims 6 and 1. Panwar further teaches that when a processor sleeps and releases its resources, it releases the instruction queue by flushing its instructions (Column 8, Lines 33-44), but Panwar does not specifically teach what other resources are released. However, Rodgers teaches particular resources that are relinquished, including registers from a register pool, entries from a store buffer, and entries in a re-order buffer (Page 4, Paragraph [0047]). One of ordinary skill in the art at the time of the invention

would have looked to available art to determine what additional resources utilized by a processor could be relinquished for the benefit of other processors. Finding Rodgers, it would have been obvious to have relinquished the registers, store buffer, and re-order buffer as taught by Rodgers, as well as the instruction queue as taught by Panwar.

27. As for Claim 17, Emer and Panwar teach all of the limitations inherited from Claims 15 and 13. Panwar further teaches that when a processor sleeps and releases its resources, it releases the instruction queue by flushing its instructions (Column 8, Lines 33-44), but Panwar does not specifically teach what other resources are released. However, Rodgers teaches particular resources that are relinquished, including registers from a register pool, entries from a store buffer, and entries in a re-order buffer (Page 4, Paragraph [0047]). One of ordinary skill in the art at the time of the invention would have looked to available art to determine what additional resources utilized by a processor could be relinquished for the benefit of other processors. Finding Rodgers, it would have been obvious to have relinquished the registers, store buffer, and re-order buffer as taught by Rodgers, as well as the instruction queue as taught by Panwar.

Response to Arguments

28. Applicant's arguments, see Pages 2-3, filed 22 August 2005, with respect to the rejection(s) of claim(s) 1-27 under 35 USC 102 and 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

However, upon further consideration, a new ground(s) of rejection is made in view of Emer, Ven, Panwar, and Rodgers.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy S. Cerullo whose telephone number is (571) 272-3634. The examiner can normally be reached on Monday - Thursday, 8:00-4:00; Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JSC

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SUPERVISORY PATENT EXAMINER
10/24/05